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#2 ((back annotation and simulat*)<in>metadata)

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#4 ((back annotation and simulat* and pre-layout)<in>metadata)

#5 ((back annotation and simulation and node?)<in>metadata)

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» Key

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **Rapid and accurate timing simulation of radiation-hardened digital microelectron**
Brothers, C.P., Jr.; Mehalic, M.A.;
Aerospace and Electronics Conference, 1994. NAECON 1994., Proceedings of the IEE
23-27 May 1994 Page(s):378 - 385 vol.1
AbstractPlus | Full Text: PDF(660 KB) IEEE CNF

2. **The University of Pennsylvania integrated circuit design environment**
Ekenberg, T.;
Nuclear Science Symposium and Medical Imaging Conference, 1994., 1994 IEEE Con
Volume 1, 30 Oct.-5 Nov. 1994 Page(s):25 - 29 vol.1
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3. **OLIVIA: object oriented logic simulation implementing the VITAL standard**
Fleischmann, J.; Schlagenhaft, R.; Peller, M.; Frohlich, N.;
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13-15 March 1997 Page(s):51 - 56
AbstractPlus | Full Text: PDF(508 KB) IEEE CNF

4. **Parametric timing and power macromodels for high level simulation of low-swing**
Bertozzi, D.; Benini, L.; Ricco, B.;
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AbstractPlus | Full Text: PDF(651 KB) IEEE CNF

5. **Execution-time profiling for multiple-process behavioral synthesis**
Adams, J.K.; Miller, J.A.; Thomas, D.E.;
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings.,
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2-4 Oct. 1995 Page(s):144 - 149
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6. **Biologically-inspired digital circuit for a self-organising neural network**
Perez, M.A.J.; Luque, W.M.; Damiani, F.;
Devices, Circuits and Systems, 1998. Proceedings of the 1998 Second IEEE Internatio
Conference on
2-4 March 1998 Page(s):172 - 177

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7. **JiffyTune: circuit optimization using time-domain sensitivities**
Conn, A.R.; Coulman, P.K.; Haring, R.A.; Morrill, G.L.; Visweswariah, C.; Chai Wah Wu
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
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9. **Verilog simulation of Xilinx designs**
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14-16 March 1994 Page(s):93 - 100
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10. **Time-Delay Optimization of RSFQ Cells**
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Applied Superconductivity, IEEE Transactions on
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11. **An integrated CAD environment for system design**
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12. **Interconnect and output driver modeling of high speed designs**
Xrao-Ming Xiong; Chung-kuan Cheng;
ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International
27 Sept.-1 Oct. 1993 Page(s):507 - 510
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13. **Verilog library development using Cadence Central Delay Calculator**
Nguyen, P.X.;
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Design, Automation and Test in Europe Conference and Exhibition, 2003
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AbstractPlus | Full Text: PDF(354 KB) IEEE CNF

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Martinez, M.A.; Polkinghorn, R.W.;
SOS/SOI Technology Workshop, 1988. Proceedings., 1988 IEEE
3-5 Oct. 1988 Page(s):71
AbstractPlus | Full Text: PDF(32 KB) IEEE CNF

☐ **16. Detailed comparison of dependability analyses performed at RT and gate levels**
Ammari, A.; Leveugle, R.; Sonza-Reorda, M.; Violante, M.;
Defect and Fault Tolerance in VLSI Systems, 2003. Proceedings. 18th IEEE Internatio
on
3-5 Nov. 2003 Page(s):336 - 343
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☐ **17. A mixed signal CMOS readout chain for imaging spectroscopic pixel X-ray detec**
Kapnistis, C.; Misiakos, K.; Haralabidis, N.;
Electronics, Circuits and Systems, 1998 IEEE International Conference on
Volume 1, 7-10 Sept. 1998 Page(s):405 - 408 vol.1
AbstractPlus | Full Text: PDF(280 KB) IEEE CNF

Results for **"((back annotation and simulat* and pre-layout)<in>metadata)"**
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((back annotation and simulation and node?)<in>metadata)

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Display Format: Citation Citation & Abstract

» Key

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IEE JNL	IEE Journal or Magazine
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1988. (INZZ) An introduction to software tools for the design of application specific integrated circuits.

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1988. (INZZ) A system for critical path analysis based on **back annotation** and distributed interconnect impedance models.

☐ 15 display full document

1987. (INZZ) The role of personal workstations in gate array design.

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1985. (INZZ) EDIF breaks CAE/CAD compatibility barrier.

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1985. (INZZ) An integrated semicustom design system.

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1989. (INZZ) Design analog ICs with CAE/CAD system.

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INSPEC - 1969 to date (INZZ)

Accession number & update
3581098, B90022013, C90022699; 900000.

Title
Design analog ICs with CAE/CAD system.

Author(s)
Goodenough-F.

Source
Electronic-Design (USA), vol.37, no.26, p.75-80, 28 Dec. 1989.

CODEN
ELODAW.

ISSN
ISSN: 0013-4872.

Publication year
1989.

Language
EN.

Publication type
J Journal Paper.

Treatment codes
P Practical.

Abstract
Artist is the first CAE/CAD tool that one can design a complete analog IC with from schematic capture through **layout,** design verification, and **back annotation** of the **parasitic** capacitances resulting from chip **layout,** to the schematic net list for resimulation. Between capture and resimulation, this highly interactive toolset performs Spice simulations and displays the results; analyzes and further processes those results; assists in chip **layout;** and verifies the design by performing engineering and design rule checks (ERCs/DRCs) as well as checking the **layout** vs. the schematic (LVS). Moreover, Artist is hierarchical, which means that from schematic capture until moving to **back annotation,** one can define the parts of the circuit at the device level (resistor, capacitor, transistor), block level (op amp, comparator), or functional level (filter or equation). (0 refs).

Descriptors
analogue-circuits; CAD-CAM; circuit-CAD; digital-simulation.

Keywords
engineering rule checks; analog ICs; CAECAD system; Artist; schematic capture; **layout;** design

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INSPEC - 1969 to date (INZZ)

Accession number & update
3780170, B91000844, C91003094; 910100.

Title
Simplified design of ASICs.

Author(s)
Gajani-S.

Author affiliation
ES2-Agrate-Brianza, Italy.

Source
Elettronica-Oggi (Italy), no.106, p.132-48, 15 Sept. 1990.

CODEN
ELOGDA.

ISSN
ISSN: 0391-6391.

Publication year
1990.

Language
IT.

Publication type
J Journal Paper.

Treatment codes
P Practical.

Abstract
Defines the steps in the design of an ASIC, namely: schematic entry, **extraction** of the netlist, **simulation,** placing and routing (eventually with **back annotation),** layout, and generation of the test program, and explains their nature. It then describes the Solo 1XXX Design Manager program by means of which these operations can be carried out in a logical manner and without errors. (0 refs).

Descriptors
application-specific-integrated-circuits; circuit-layout-CAD; logic-CAD; software-packages.

Keywords
placement; ASICs; schematic entry; netlist; **simulation;** routing; **back annotation;** layout; test program; Solo 1XXX Design Manager program.

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1 A Fully Qualified Top-Down and Bottom-Up Mixed-Signal Design Flow for Non Volatile Memories Technologies

Pierluigi Daglio, Carlo Roma

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2**

Full text available: pdf(714.21 KB) Publisher Site

Additional Information: full citation, abstract

The wide range and rapid increase in the complexity of EDA tools demand proven and safe design flows. This paper presents a complete and fully qualified mixed-signal top-down design flow for non volatile memory applications. It has been successfully applied to an Embedded Flash Macrocell based design as well as to a 14-bit analog/digital converter with digital non linearity compensation manufactured in 0.18um proprietary flash technology. One remarkable feature of the proposed methodology is the ...

2 A practical approach to static signal electromigration analysis

Nagaraj NS, Frank Cano, Haldun Haznedar, Duane Young

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(189.87 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

It is commonly thought that sweep-back effects would make electromigration (EM) a non-issue in signal lines. However this is only the case when the shape of the positive and negative current pulses are closely matched. Moreover, as performance pressures increase, the peak current values are exceeding the range for which electromigration models are valid. Thus, during the design of TI's TMS320c6201 DSP chip, it was determined that limits needed to be placed on the current densities in signal ...

3 A flat, timing-driven design system for a high-performance CMOS processor chipset

J. Koehl, U. Baur, T. Ludwig, B. Kick, T. Pflueger

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(155.54 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

We describe the methodology used for the design of the CMOS processor chipset used in

the IBM S/390 Parallel Enterprise Server - Generation 3. The majority of the logic is implemented by standard cell elements placed and routed flat, using timing-driven techniques. The result is a globally optimized solution without artificial floorplan boundaries. We will show that the density in terms of transistors per mm2 is comparable to the most advanced custom designs and that the impact of interconnect d ...

4 Layout extraction and verification methodology CMOS I/O circuits

Tong Li, Sung-Mo Kang

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(475.94 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

This paper presents a layout extraction and verification methodology which targets reliability-driven I/O design for CMOS VLSI chip, specifically to guard against electrostatic discharge (ESD) stress and latchup. We propose a new device extraction approach to identify devices commonly used in CMOS I/O circuits including MOS transistors, field transistors, diffusion and well resistors, diodes and silicon controlled rectifiers (SCRs), etc. Unlike other extractors, our extractor identifies cir ...

Keywords: congestion, global routing, quadratic placement, relaxed pins, routing models, supply-demand

5 Combined topological and functionality based delay estimation using a layout-driven approach for high level applications

Champaka Ramachandran, Fadi J. Kurdahi

November 1992 **Proceedings of the conference on European design automation**

Full text available: pdf(854.38 KB) Additional Information: full citation, references, citings, index terms

6 Session 3: From the Trenches (invited): The scaling challenge: can correct-by-construction design help?

Prashant Saxena, Noel Menezes, Pasquale Cocchini, Desmond A. Kirkpatrick

April 2003 **Proceedings of the 2003 international symposium on Physical design**

Full text available: pdf(294.86 KB) Additional Information: full citation, abstract, references, citings, index terms

We present the results of scaling studies in the context of typical block-level wiring distributions, and study the impact of the identified trends on the post-RTL design process. In particular, we look at the implications of exponentially increasing repeater and clocked repeater counts on the algorithms and methodologies used for logic synthesis, technology mapping, layout, and full-chip assembly, and identify several new research problems relevant to future designs. Next, we introduce the basi ...

Keywords: clocked repeaters, correct-by-construction design, design fabrics, interconnect, logic synthesis, placement, post-RTL design, repeaters, routing, scaling, technology mapping

7 VHDL-based design and design methodology for reusable high performance direct digital requency synthesizers

Ireneusz Janiszewski, Bernhard Hoppe, Hermann Meuth

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(226.11 KB) Additional Information: full citation, abstract, references, index terms

Design methodologies for high performance Direct Digital Fre-quen--cy Synthesizers (DDFS) are described. Traditional look-up tab-les (LUT) for sine and co-sine are merged with CORDIC-inter-po---la--tion into a hybrid architecture. This implements DDFS-sys-tems with high resolution without being specific to a particular tar-get technology. Amplitude constants were obtained from ma-the-matical trigonometric functions of the IEEE math_real pack-age. These constants were then written via simula ...

Keywords: CORDIC algorithm, HDL-based design, design optimization and reuse, direct frequency synthesis

8 (Special session) embedded tutorial: RF modeling and design methodology: RF design methodologies bridging system-IC-module design

Robert A. Mullen
January 2004

Full text available: pdf(538.14 KB) Publisher Site Additional Information: full citation, abstract, references

There has been a long-standing need to link the RF design domains into a connected, common design environment. Such a methodology is possible through implementing system-level behavioral models with different levels of abstraction that can be modeled or co-simulated at the IC circuit level. At module or board design, it is possible to link and simulate multiple chips with board-level components and parastics in an RFIC design environment.With today's more complex IC designs that are heading towa ...

9 The role of timing verification in layout synthesis

Jacques Benkoski, Andrzej J. Strojwas
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Full text available: pdf(889.07 KB) Additional Information: full citation, references, citings, index terms

10 High-level simulation of substrate noise generation including power supply noise coupling

Marc van Heijningen, Mustafa Badaroglu, Stéphane Donnay, Marc Engels, Ivo Bolsens
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(114.20 KB) Additional Information: full citation, abstract, references, citings, index terms

Substrate noise caused by large digital circuits will degrade the performance of analog circuits located on the same substrate. To simulate this performance degradation, the total amount of generated substrate noise must be known. Simulating substrate noise generated by large digital circuits is however not feasible with existing circuit simulators and detailed substrate models due to the long simulation times and high memory requirements. We have developed a methodology to simulate this su ...

11 A new concept for accurate modeling of VLSI interconnections and its application for timing simulation

B. Wunder, G. Lehmann, K. Müller-Glaser
September 1996 **Proceedings of the conference on European design automation**

Full text available: pdf(415.21 KB) Additional Information: full citation, references, index terms

12 Design methods for manufacturability enhancements: Advanced timing analysis based on post-OPC extraction of critical dimensions
Jie Yang, Luigi Capodieci, Dennis Sylvester
June 2005 **Proceedings of the 42nd annual conference on Design automation**

Full text available: pdf(998.62 KB) Additional Information: full citation, abstract, references, index terms

While performance specifications are verified before sign-off for a modern nanometer scale design, extensive application of optical proximity correction substantially alters the layout introducing systematic variations to the simulated and verified performance. As a result, actual on-silicon chip performance is quite different from sign-off expectations. This paper presents a new methodology to provide better estimates of on-silicon performance. The technique relies on the extraction of residual ...

Keywords: OPC, design flow, layout, process CD

13 Electromagnetic modeling and signal integrity simulation of power/ground networks in high speed digital packages and printed circuit boards
Frank Y. Yuan
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(275.46 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

The electromagnetic modeling and parameter extraction of digital packages and PCB boards for system signal integrity applications are presented. A systematic approach to analyze complex power/ground structures and simulate their effects on digital systems is developed. First, an integral equation boundary element algorithm is applied to the electromagnetic modeling of the PCB structures. Then, equivalent circuits of the power/ground networks are extracted from the EM solution. In an integra ...

Keywords: custom sizing, migration, timing optimazation

14 Mixed-signal design and simulation: A 16-bit mixed-signal microsystem with integrated CMOS-MEMS clock reference
Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadi H. Gebara, Keith L. Kraver, Matthew R. Guthaus, Richard B. Brown
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(793.60 KB) Additional Information: full citation, abstract, references, citings, index terms

In this work, we report on an unprecedented design where digital, analog, and MEMS technologies are combined to realize a general-purpose single-chip CMOS microsystem. The convergence of these technologies has enabled the development of a low power, portable microinstrument ideally suited for controlling environmental and bio-implantable sensors.

Keywords: ADC, MEMS, PGA, SD, SoC, clock generation, design methodology, inductor, low power, low voltage analog, microcontroller, microsystem, mixed-signal, system-on-chip, varactor

15 Layout tools for analog ICs and mixed-signal SoCs: a survey
Rob A. Rutenbar, John M. Cohn
May 2000 **Proceedings of the 2000 international symposium on Physical design**

Full text available: pdf(247.03 KB) Additional Information: full citation, references

16 Timing abstraction: Automated timing model generation
Ajay J. Daga, Loa Mize, Subramanyam Sripada, Chris Wolff, Qiuyang Wu
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(260.13 KB) Additional Information: full citation, abstract, references, index terms

The automated generation of timing models from gate-level netlists facilitates IP reuse and dramatically improves chip-level STA runtime in a hierarchical design flow. In this paper we discuss two different approaches to model generation, the design flows they lend themselves to and results from the application of these model generation solutions to large customer designs.

Keywords: EDA, model generation, static timing analysis

17 EMI-noise analysis under ASIC design environment
Sachio Hayashi, Masaaki Yamada
April 1999 **Proceedings of the 1999 international symposium on Physical design**

Full text available: pdf(912.47 KB) Additional Information: full citation, references, index terms

18 Power minimization in IC design: principles and applications
Massoud Pedram
January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

19 Session 12: Parametric timing and power macromodels for high level simulation of low-swing interconnects
Davide Bertozzi, Luca Benini, Bruno Ricco'
August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available: pdf(217.21 KB) Additional Information: full citation, abstract, references, index terms

The impact of global on-chip interconnections on power consumption and speed of integrated circuits is becoming a serious concern. Designers need therefore to quickly estimate how performance and power are affected by a given choice of the interconnection

parameters (length, voltage swing, driver and receiver schematics and sizing). This work focuses on the entire communication channel (driver, interconnect, receiver), and provides high level parametric VHDL simulation models for low-swing signa ...

Keywords: delay, interconnect, low-swing, macromodel, power

20 Optimization of custom MOS circuits by transistor sizing

Andrew R. Conn, Paula K. Coulman, Ruud A. Haring, Gregory L. Morrill, Chandu Visweswariah
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(68.85 KB) Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

Optimization of a circuit by transistor sizing is often a slow, tedious and iterative manual process which relies on designer intuition. Circuit simulation is carried out in the inner loop of this tuning procedure. Automating the transistor sizing process is an important step towards being able to rapidly design high-performance, custom circuits. JiffyTune is a new circuit optimization tool that automates the tuning task. Delay, rise/fall time, area and power targets are accommodated. Each (weig ...

Keywords: Circuits, transistor sizing, optimization, simulation, gradients.

WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Monday, June 27, 2005

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ	
☐	L7	L4 and pre-layout near5 simulation	3
☐	L6	L4 and pre-layout	8
☐	L5	L4 and parasitic near5 element?	5
☐	L4	L2 and nodes	25
☐	L3	L2 and (back annotation near simulation)	0
☐	L2	back annotation and simulation and parasitic and extraction	40
☐	L1	kuzuma.in. and back annotation and simulation	1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 20020013688 A1

L1: Entry 1 of 1 File: PGPB Jan 31, 2002

PGPUB-DOCUMENT-NUMBER: 20020013688
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020013688 A1

TITLE: Back annotation apparatus for carrying out a simulation based on the extraction result in regard to parasitic elements

PUBLICATION-DATE: January 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kuzuma, Hiroyuki	Hyogo		JP	
Yamasaki, Terutoshi	Hyogo		JP	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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Term	Documents
KUZUMA	11
KUZUMAS	0
BACK	1594712
BACKS	24263
ANNOTATION	8192
ANNOTATIONS	5216
SIMULATION	85376
SIMULATIONS	28315
((KUZUMA.IN.) AND (BACK ADJ ANNOTATION) AND SIMULATION).PGPB,USPT.	1
(KUZUMA.IN. AND BACK ANNOTATION AND SIMULATION).PGPB,USPT.	1

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Search Results - Record(s) 1 through 5 of 5 returned.

☐ 1. Document ID: US 20040049747 A1

L5: Entry 1 of 5 File: PGPB Mar 11, 2004

PGPUB-DOCUMENT-NUMBER: 20040049747
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040049747 A1

TITLE: Verification apparatus

PUBLICATION-DATE: March 11, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yamasaki, Terutoshi	Tokyo		JP	
Harada, Masaaki	Tokyo		JP	
Natsume, Keiko	Tokyo		JP	

US-CL-CURRENT: 716/4; 716/12, 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20020013688 A1

L5: Entry 2 of 5 File: PGPB Jan 31, 2002

PGPUB-DOCUMENT-NUMBER: 20020013688
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020013688 A1

TITLE: Back annotation apparatus for carrying out a simulation based on the extraction result in regard to parasitic elements

PUBLICATION-DATE: January 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kuzuma, Hiroyuki	Hyogo		JP	
Yamasaki, Terutoshi	Hyogo		JP	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6874132 B1

L5: Entry 3 of 5 File: USPT Mar 29, 2005

US-PAT-NO: 6874132
DOCUMENT-IDENTIFIER: US 6874132 B1

TITLE: Efficient extractor for post-layout simulation on memories

DATE-ISSUED: March 29, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bhamidipaty; Achyutram	San Jose	CA		

US-CL-CURRENT: 716/1; 716/18, 716/4, 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 4. Document ID: US 5715170 A

L5: Entry 4 of 5 File: USPT Feb 3, 1998

US-PAT-NO: 5715170
DOCUMENT-IDENTIFIER: US 5715170 A

TITLE: Apparatus for forming input data for a logic simulator

DATE-ISSUED: February 3, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nakamori; Tutomu	Kawasaki			JP

US-CL-CURRENT: 703/19; 703/15

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 5. Document ID: US 5452224 A

L5: Entry 5 of 5 File: USPT Sep 19, 1995

US-PAT-NO: 5452224
DOCUMENT-IDENTIFIER: US 5452224 A

TITLE: Method of computing multi-conductor parasitic capacitances for VLSI circuits

DATE-ISSUED: September 19, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Smith, Jr.; William R.	Laguna Niguel	CA		
Brodie; Richard A.	Oceanside	CA		
Beaven; Michael W.	West Lafayette	IN		

US-CL-CURRENT: 716/19; 706/921

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Term	Documents
PARASITIC	76032
PARASITICS	3790
ELEMENT?	0
ELEMENTA	30
ELEMENTB	8
ELEMENTC	2
ELEMENTD	5
ELEMENTE	145
ELEMENTF	3
ELEMENTI	8
ELEMENTK	1
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☐ 1. Document ID: US 20040049747 A1

L6: Entry 1 of 8 File: PGPB Mar 11, 2004

PGPUB-DOCUMENT-NUMBER: 20040049747
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040049747 A1

TITLE: Verification apparatus

PUBLICATION-DATE: March 11, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yamasaki, Terutoshi	Tokyo		JP	
Harada, Masaaki	Tokyo		JP	
Natsume, Keiko	Tokyo		JP	

US-CL-CURRENT: 716/4; 716/12, 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20020013688 A1

L6: Entry 2 of 8 File: PGPB Jan 31, 2002

PGPUB-DOCUMENT-NUMBER: 20020013688
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020013688 A1

TITLE: Back annotation apparatus for carrying out a simulation based on the extraction result in regard to parasitic elements

PUBLICATION-DATE: January 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kuzuma, Hiroyuki	Hyogo		JP	
Yamasaki, Terutoshi	Hyogo		JP	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6874132 B1

L6: Entry 3 of 8 File: USPT Mar 29, 2005

US-PAT-NO: 6874132
DOCUMENT-IDENTIFIER: US 6874132 B1

TITLE: Efficient extractor for post-layout simulation on memories

DATE-ISSUED: March 29, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bhamidipaty; Achyutram	San Jose	CA		

US-CL-CURRENT: 716/1; 716/18, 716/4, 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 4. Document ID: US 6212665 B1

L6: Entry 4 of 8 File: USPT Apr 3, 2001

US-PAT-NO: 6212665
DOCUMENT-IDENTIFIER: US 6212665 B1
**** See image for Certificate of Correction ****

TITLE: Efficient power analysis method for logic cells with many output switchings

DATE-ISSUED: April 3, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Zarkesh; Amir M.	Tarzana	CA		
Chen; Haizhou	Goleta	CA		

US-CL-CURRENT: 716/4; 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 5. Document ID: US 5933356 A

L6: Entry 5 of 8 File: USPT Aug 3, 1999

US-PAT-NO: 5933356
DOCUMENT-IDENTIFIER: US 5933356 A

TITLE: Method and system for creating and verifying structural logic model of electronic design from behavioral description, including generation of logic and timing models

DATE-ISSUED: August 3, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA		
Dangelo; Carlos	Los Gatos	CA		
Bair; Owen S.	Saratoga	CA		

US-CL-CURRENT: 703/15; 716/12, 716/6, 716/8

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 6. Document ID: US 5880971 A

L6: Entry 6 of 8 File: USPT Mar 9, 1999

US-PAT-NO: 5880971
DOCUMENT-IDENTIFIER: US 5880971 A

TITLE: Methodology for deriving executable low-level structural descriptions and valid physical implementations of circuits and systems from semantic specifications and descriptions thereof

DATE-ISSUED: March 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dangelo; Carlos	San Jose	CA		
Nagasamy; Vijay Kumar	Mountain View	CA		
Bootehsaz; Ahsan	Santa Clara	CA		
Rajan; Sreeranga Prasannakumar	Sunnyvale	CA		

US-CL-CURRENT: 716/6

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 7. Document ID: US 5572437 A

L6: Entry 7 of 8 File: USPT Nov 5, 1996

US-PAT-NO: 5572437
DOCUMENT-IDENTIFIER: US 5572437 A

TITLE: Method and system for creating and verifying structural logic model of electronic design from behavioral description, including generation of logic and timing models

DATE-ISSUED: November 5, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA		
Dangelo; Carlos	Los Gatos	CA		
Bair; Owen S.	Sarotoga	CA		

US-CL-CURRENT: 716/18; 703/13, 716/6

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWMC | Draw. De

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☐ 8. Document ID: US 5526277 A

L6: Entry 8 of 8 File: USPT Jun 11, 1996

US-PAT-NO: 5526277
DOCUMENT-IDENTIFIER: US 5526277 A

TITLE: ECAD system for deriving executable low-level structural descriptions and valid physical implementations of circuits and systems from high-level semantic descriptions thereof

DATE-ISSUED: June 11, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dangelo; Carlos	San Jose	CA		
Nagasamy; Vijay K.	Mountain View	CA		
Bootehsaz; Ahsan	Santa Clara	CA		
Rajan; Sreeranga P.	Sunnyvale	CA		

US-CL-CURRENT: 716/3; 716/11, 716/18, 716/7

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWMC | Draw. De

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Term	Documents
PRE-LAYOUT	134
PRE-LAYOUTS	0
(PRE-LAYOUT AND 4).PGPB,USPT.	8
(L4 AND PRE-LAYOUT).PGPB,USPT.	8

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 20040049747 A1

L7: Entry 1 of 3 File: PGPB Mar 11, 2004

PGPUB-DOCUMENT-NUMBER: 20040049747
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040049747 A1

TITLE: Verification apparatus

PUBLICATION-DATE: March 11, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yamasaki, Terutoshi	Tokyo		JP	
Harada, Masaaki	Tokyo		JP	
Natsume, Keiko	Tokyo		JP	

US-CL-CURRENT: 716/4; 716/12, 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20020013688 A1

L7: Entry 2 of 3 File: PGPB Jan 31, 2002

PGPUB-DOCUMENT-NUMBER: 20020013688
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020013688 A1

TITLE: Back annotation apparatus for carrying out a simulation based on the extraction result in regard to parasitic elements

PUBLICATION-DATE: January 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kuzuma, Hiroyuki	Hyogo		JP	
Yamasaki, Terutoshi	Hyogo		JP	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6874132 B1

L7: Entry 3 of 3 File: USPT Mar 29, 2005

US-PAT-NO: 6874132
DOCUMENT-IDENTIFIER: US 6874132 B1

TITLE: Efficient extractor for post-layout simulation on memories

DATE-ISSUED: March 29, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bhamidipaty; Achyutram	San Jose	CA		

US-CL-CURRENT: 716/1; 716/18, 716/4, 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
PRE-LAYOUT	134
PRE-LAYOUTS	0
SIMULATION	85376
SIMULATIONS	28315
((PRE-LAYOUT NEAR5 SIMULATION) AND 4).PGPB,USPT.	3
(L4 AND PRE-LAYOUT NEAR5 SIMULATION).PGPB,USPT.	3

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